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download . . Tutorial: A: The answer is
"Yes". Somebody does find it. . (1) Field of the
Invention The present invention relates to semiconductor
memory devices, and more particularly to a
semiconductor memory device, such as a Dynamic
Random Access Memory (DRAM) which is designed to
have a memory core integrated on one semiconductor
substrate, wherein a series of masking steps are
performed before forming a series of auxiliary MOS
transistor structures. (2) Description of the Prior Art
Semiconductor memory devices such as DRAMs are
typically made of multiple levels of metal
interconnections, which are formed using an interlevel
dielectric layer and chemical-mechanical polishing. The
interlevel dielectric layer is typically formed over a
device substrate such as a silicon wafer, wherein device
elements and other circuit components are formed. The
metal interconnections are typically formed within the
interlevel dielectric layer, and are used to provide

electrical connections between various circuit components. Conventional technology has a number of limitations, which may be traced to the use of large area metal interconnections. Because the metal interconnections are formed using conventional lithographic processing (for example, using a photoresist layer and subsequent processing by etching), the minimum dimensions of the metal interconnections are limited by the resolution of the photolithography process. For example, a device comprising metal interconnections having a minimum size of 0.5 micrometers cannot be readily manufactured using conventional lithographic techniques. A related problem arising with the use of large area metal interconnections is that the metal interconnections may cross over or under the gate electrode of a transistor, as well as over the isolation regions between active devices. When metal interconnections are formed over the isolation regions, or over the gate electrode of a transistor, circuit malfunctions may result. Moreover, the process of chemical-mechanical polishing to smooth the interlevel dielectric layer is a time-

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